THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 19

UNITED STATES PATENT AND TRADEMARK OFFICE

_____

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

_____

Ex parte PRADEEP S. SINDHU, JEAN-MARC FRAILONG
and JEAN A. GASTINEL

_____

Appeal No. 95-4096
Application No. 08/188,660[1]

_____

ON BRIEF

_____

Before HAIRSTON, KRASS and FLEMING, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

---

[1] Application for patent filed January 27, 1994. According to appellants, this application is a continuation of Application 07/620,508, filed November 30, 1990, now abandoned.

This is a decision on appeal from the final rejection of claims 2 through 4, the only claims pending in the application.

The invention is directed to a packet switched bus for carrying out memory transactions in a shared memory multiprocessor. The packet switched bus handles multiple memory transactions (e.g., read/write) in a time overlapping manner, with each "request" followed at some later time by a "reply." These request/reply pairs are logically disassociated, unlike in circuit switched bus systems which involve master/slave relationships between the transaction requester and the responders. In those systems, the master maintains control of the bus from the time control is granted until it receives a reply to its request.

The instant invention uses cache memory to enable each of the processors and the I/O devices to cache addresses locally that the devices are likely to be writing data to and/or reading data from. Since this may mean that there could be multiple copies of a given address at various sites within the memory system, there must be some provision for avoiding the potential problems of inconsistent data being employed. While

the problem has been said to have been solved in circuit switched bus systems by write back and invalidate data consistency techniques, the instant invention is said to solve the problem in packet switched bus systems by the use of synchronous buses (shown as buses 15a-15i in Figure 1). By a more efficient use of the available bus bandwidth, the buses permit transactions to be performed using packets of differing length, packet lengths being determined by logical requirements of the transactions rather than by the timing requirements of the bus.

Independent claim 2 is reproduced as follows:

2. In a shared memory multiprocessor having a main memory, a plurality of processors, I/O devices, and respective cache memories coupled to said processors and to said I/O devices; the improvement comprising

a packet switched bus coupled to said main memory and to said cache memories for transferring commands, memory addresses, and data therebetween in compliance with selected ones of a predefined set of memory transactions, including transactions that cause multiple copies of at least some of said data to be updated at different times under the control of different ones of said processors;

each of said transactions being composed of a request packet followed at an indeterminate later time by a reply packet, thereby enabling the request and reply packets for multiple transactions to be time interleaved on said bus;

said transactions being selected to enforce a consistency protocol that ensures that all of said processors and all of said I/O devices have access to consistent values for all data stored in said cache memories, including all data represented by said multiple copies.

The examiner relies on the following references:

Baxter et al. (Baxter)	4,535,448	Aug. 13, 1985
Dashiell et al. (Dashiell)	4,843,542	Jun. 27, 1989

Claims 2 through 4 stand rejected under 35 U.S.C. 112, second paragraph, as being indefinite. Claims 2 through 4 stand further rejected under 35 U.S.C. 103 as unpatentable over Dashiell in view of Baxter.

Rather than reiterate the arguments of appellants and the examiner, reference is made to the briefs and answer for the respective details thereof.

OPINION

Turning first to the rejection of claims 2 through 4 under 35 U.S.C. 112, second paragraph, we will not sustain this rejection.

The examiner rejects the claims as being "functional" and not being "supported by recitation of sufficient structure to warrant the presence of the functional language" [answer- page 3]. We disagree.

We note that the examiner cites MPEP 706.03(c) as authority for a rejection based on claims being "functional." Reference to this section of the MPEP, however, indicates that the section refers to rejections under the *first* paragraph of 35 U.S.C. 112 which would include lack of best mode, written description and enablement problems. There is nothing therein giving the examiner authority to reject a claim as being "functional."

In any event, our review of instant claims 2 through 4 reveals nothing therein which would be considered indefinite within the meaning of 35 U.S.C. 112, second paragraph. The claims recite the general structure which comprises a shared memory multiprocessor system, such as a main memory, a plurality of processors, I/O devices and cache memories. The claims further recite a packet switched bus coupled to the main memory and to the cache memories for transferring commands, memory addresses and data between the memories in

accordance with selected ones of a predefined set of memory transactions. Some of these transactions may cause multiple copies of at least some of the data to be updated at different times. The remainder of the claims contain recitations as to what comprises the transactions and how the transactions are selected as well as more details as to the request and reply packets.

It may be that the claim language is rather broad but the examiner should not confuse breadth with indefiniteness. See In re Miller, 441 F.2d 689, 693, 169 USPQ 597, 600 (CCPA 1971).

We now turn to the rejection based on prior art. We will not sustain this rejection as it is our view that the examiner has not established a prima facie case of obviousness with regard to the claimed subject matter.

The examiner cites Dashiell for the teaching of a shared memory multiprocessor having a plurality of processors, I/O devices and cache memories connected to a bus. However, as the examiner recognizes, Dashiell does not disclose that the bus is a packet switched bus, as claimed by appellants. Accordingly, the examiner relies on Baxter for the suggestion

of a desirability to use a packet switched bus for bursty or high speed data transfer and optimum utilization of resources. The examiner then concludes that it would have been obvious to use a packet switched bus in Dashiell in order "to achieve efficient bursty or high speed data transfer and optimizing the utilization of resources as suggested by Baxter" [answer-page 5].

It is our view that the skilled artisan would not have been led to substitute a packet switched bus for the MBUS 29 of Dashiell. Dashiell discloses a very specific system for maintaining data consistency among distributed processors wherein a cache memory associated with each processor accesses data from another cache, if needed, or from real memory. When a processor writes into a data word in the cache, the cache will update all other caches that share the data before allowing the write to the local cache. Thus, once a cache gets control of the bus in Dashiell, it does not relinquish control until all other caches have been updated, at which time the cache releases the MBUS and writes data into its own cell, setting its own master flag and updating its own LRU stack [column 9, lines 23-28].

If one were to substitute, for whatever reason, a packet-switched bus for the MBUS of Dashiell, Dashiell's operation would appear to be inoperable. The data consistency sought by Dashiell would not be achieved by the use of a packet-switched bus since, as explained by Baxter, at column 5, lines 28-31, "a packet-switched bus is a bus whose bandwidth is allocated on a demand basis, as opposed to a circuit-switched bus, whose bandwidth is allocated for the duration of the connection." Since the bus of Dashiell is not a packet-switched bus, extensive modification of Dashiell would be necessary in order to derive any operable system, such modification constituting invention itself, wherein data consistency is maintained while employing a packet-switched bus. This, of course, is appellants' invention.

Further, since Baxter is not concerned at all with the use of cache memories or the maintenance of data consistency, there seems to be no reason for the artisan to have been led to employ the packet-switched bus of Baxter in a shared memory multiprocessor system for maintaining data consistency. Where is the suggestion to so employ Baxter's packet-switched bus? A mere reference, by Baxter [column 1, lines 16-17], to such a

bus being an efficient transfer medium for bursty, or high speed, data appears to be a weak motivation for attempting to use a packet-switched bus in Dashiell when Dashiell does not indicate that the data therein is high speed data of the type of interest in Baxter and there is no indication that the system of Dashiell would work with a packet-switched bus. The examiner fails to take into account that the completely different types of buses do not easily permit the substitution of one for the other without an attendant, more-than-routine, modification of other parts of the system.

Instant claim 2 clearly calls for the transactions comprising "a request packet followed at an indeterminate later time by a reply packet..." Clearly, the Dashiell system operates in a completely different manner. There is no request packet therein which is followed at an indeterminate later time by a reply packet.

The examiner's decision rejecting claims 2 through 4 under both 35 U.S.C. 112, second paragraph, and under 35 U.S.C. 103 is reversed.

REVERSED

KENNETH W. HAIRSTON)
Administrative Patent Judge)
)
)
)
ERROL A. KRASS) BOARD OF PATENT
Administrative Patent Judge) APPEALS AND
) INTERFERENCES
)
)
MICHAEL R. FLEMING)
Administrative Patent Judge)

Appeal No. 95-4096
Application No. 08/188,660

Ronald Zibelli
Xerox Corporation
Xerox Square - 020
Rochester, NY 14644